ORTEC®

# Delays/Gate and Delay Generators/ Logic Modules/Linear Gates

## Delays

In experiments involving several sources of analog and logic signals, the signals from different paths usually must be aligned to arrive simultaneously at the decision points. This is the function of delay modules. For analog signals the pulse amplitude information must be preserved. Consequently, coaxial cables or lumped-parameter delay lines are used to generate the delay.

With logic pulses, three methods can be used. For short delays, coaxial cables can be employed. A more compact solution uses lumped-parameter delays with logic gates acting as buffers between the many delay sections. These first two solutions minimize the dead time following each pulse. If dead time is not a problem, the simplest method of achieving long delays with logic pulses is to use a "gate and delay generator." In this case, the original logic signal triggers a "one-shot" circuit. The width of the one-shot pulse sets the delay, and the trailing edge of the one-shot signal triggers the output pulse. Typically, another one-shot is used to set the width of the output pulse.

## Logic Modules

In coincidence measurements, logic signals from various parts of the experiment must often be combined to determine which events are to be accepted for analysis. Logic modules provide a flexible means of making these decisions.

## Linear Gates

When some analog signals must be blocked, and some must be selected to pass on to a subsequent instrument, a linear gate is required. Linear gates usually provide a variety of ways to use a logic pulse in blocking or passing the analog signal.

## Delay Selection Guide

| | DB463 Delay Box | 425A Nanosecond Delay |
|---|---|---|
| **Type of Signal** | Analog or logic | Analog or logic |
| **Number of Duplicate Channels** | 4 | 1 |
| **Delay Range per Channel** | 0 to 63.5 ns | 2 to 65 ns |
| **Minimum Delay Adjustment** | 0.5 ns | 1 ns |

## Gate and Delay Generator Selection Guide

| | GG8020 Octal Gate and Delay Generator | 416A Gate and Delay Generator |
|---|---|---|
| **Number of Duplicate Channels** | 8 | 1 |
| **Module Width** | NIM-1 | NIM-1 |
| **Input** | Fast negative NIM logic pulse | Slow positive NIM, or fast negative NIM logic pulse |
| **Outputs** | Fast negative NIM and TTL logic pulses | Positive and negative delayed outputs with amplitude adjustable from 2 to 10 V; delay period (+5 V); delay marker (fast negative NIM) |
| **Output Delay** | <70 ns to >10 µs | 100 ns to 110 µs |
| **Output Width** | <70 ns to >10 µs | 400 ns to 4 µs |

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## Logic Module Selection Guide

| | CO4020 Quad 4-Input Logic Unit | 414A Fast Coincidence | 418A Universal Coincidence |
|---|---|---|---|
| **Number of Duplicate Channels** | 4 | 1 | 1 |
| **Module Width** | NIM-1 | NIM-2 | NIM-1 |
| **Logic Functions** | AND, OR | AND, anti-coincidence | Majority AND, NAND |
| **Number of Inputs Per Channel** | 4 | 3 | 5 |
| **Input Level** | Fast negative NIM negative NIM | Slow positive NIM | Slow positive NIM |
| **Outputs** | TTL and Fast | Slow positive NIM | Slow positive NIM |
| **Special Features** | Adjustable output widths | Adjustable resolving time widths | Majority logic |

## Linear Gate Selection Guide

| | 426 Linear Gate | 542 Linear Gate and Stretcher |
|---|---|---|
| **Input Pulse Amplitude Range** | +200 mV to +10 V | +100 mV to +10 V |
| **Minimum and Maximum Rise Time** | <0.3 µs to dc | 0.1 to 10 µs |
| **Input Coupling** | ac-coupled with passive, symmetric BLR; can be dc-coupled | dc-coupled, or ac-coupled with active BLR |
| **Output Reshaping** | None | Input peak amplitude stretched and gated out as a rectangular output pulse |
| **Gating Functions** | Pulse pass, pulse inhibit, dc inhibit | Normally open, coincidence, anticoincidence,external strobe |

Specifications subject to change
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