

- **Fast histogramming of spectral data from CAMAC ADCs equipped with FERAbus™ readout**
- **TWO modes of operation: Monitor mode and Readout Control mode**
- **MONITOR MODE** histograms spectra from preselected ADCs in multi-parameter coincidence experiments, while listening to list-mode readouts on the FERAbus  
*Relieves the central computer of time- and memory-consuming histogramming tasks*
- **READOUT CONTROL MODE** operates as the readout controller for histogramming singles spectra from multiple ADCs  
*A powerful, cost-effective solution for multiple MCAs and high counting rates*
- **CAMAC programmable to histogram thirty-two 1k ADCs, sixteen 2k ADCs, eight 4k ADCs, four 8k ADCs, or two 16k ADCs**
- **CAMAC control of: histogramming start/stop, readout of selected segments, memory clear, ADC assignments, and FERAbus functions**



The ORTEC Model HM413 CAMAC FERAbus Histogramming Memory provides histogramming of the spectral data from ADCs equipped with the standard FERAbus™ readout port. The Model HM413 has two modes of operation: (a) the Monitor mode, and (b) the Readout Control mode. In the Monitor mode, the Model HM413 histograms spectra from pre-selected ADCs while listening to list-mode readouts on the FERAbus. This is an efficient solution for monitoring the spectra from various ADCs during a multi-parameter coincidence experiment. It relieves the data processing computer of the time-consuming and memory-consuming histogramming tasks. In the Readout Control mode, the HM413 functions as the readout controller for histogramming *singles* spectra from multiple ADCs. This is a powerful and cost-effective solution when the *singles* spectra from a large number of detectors must be analyzed at high counting rates.

The histogramming memory has a length of 32,768 channels and a capacity of 16,777,215 counts per channel (24 bits). It can be configured by CAMAC commands to histogram two 16,384-channel ADCs, four 8192-channel ADCs, eight 4096-channel ADCs, sixteen 2048-channel ADCs, or thirty-two 1024-channel ADCs. CAMAC commands assign the memory segments to histogram particular ADCs on the basis of the Virtual Station Number of the ADC

module and the Subaddress of each ADC within the module. Depending on the number of bits delivered by the ADCs, each Model HM413 serves all ADCs located in one or two ADC modules.

The Model HM413 supports all CAMAC ADCs that provide the standard FERAbus control and data output formats, as defined in the ECL Inputs/Outputs section of the Model HM413 specifications. This includes the CAMAC/FERAbus series of ORTEC ADCs and the LeCroy 4300B 16-Input ADC. All ADCs must operate in the zero-suppressed readout mode in order to provide the Virtual Station Number, the Subaddress, and the Header Word that the Model HM413 uses to identify the assigned ADCs. The Model HM413 supports both the Singles and Coincidence modes featured in the ORTEC FERAbus ADCs. The LeCroy 4300B operates only in the Coincidence mode.

In the Monitor mode, the Model HM413 simply listens to the ADC readouts occurring on the FERAbus, while the LeCroy 4301 acts as the readout controller for the list-mode readout (Fig. 1a). The WST (Write Strobe) signal on the ECL Control Bus causes the Model HM413 to read each word on the ECL Data Bus into a fast FIFO memory. This buffer memory allows the Model HM413 to track the readout of a crate full of ADCs at 100 ns per word. The Model HM413 continuously unloads the FIFO memory, and histograms only the data corresponding to its assigned ADCs.

In the Readout Control mode, the Model HM413 acts as the readout controller (Fig. 1b). This mode is used for histogramming the *singles* spectra from multiple ADCs. ADC data acquisition can be either gated by the master GATE, or ungated. The GAI gate inputs of the Model HM413 allow ECL, fast negative NIM, TTL, or slow positive NIM logic signals to be used for the master GATE input. When an ADC has data ready for readout, it generates a Readout Request (REQ) on the ECL Control Bus. The Model HM413 enables the readout by sending a Readout (REO) Signal, via a twisted-pair cable, to the Readout

Enable (REN) input of the first ADC in the readout loop. The Model HM413 reads the data from the ADC in the same way as in the Monitor mode, except that the Model HM413 accepts and generates the handshake signals that control the data transfer. When the ADC has finished its readout, it sends a PASS signal to the REN input of the next ADC. If the next ADC is not requesting a readout, it delivers a PASS signal to the REN input of the following ADC. The PASS output from the last ADC is sent to the CLI input of the Model HM413 to generate a Clear (CLR) signal on the ECL Control Bus. The CLR signal releases all ADCs to accept the next event. The CLI input connection is not required with ORTEC ADCs operating in the Singles mode, but is required for the Coincidence mode. Use of the CLI signal is mandatory for the LeCroy 4300B ADC.

CAMAC controls are provided for starting and stopping the histogramming process, for reading the contents of a selected memory segment, and for erasing the spectral data in the entire memory. These functions can be executed without interfering with the continuous operation

of the FERAbus readout, providing the F(26)-A(1) and F(24)-A(1) commands are used to start and stop data acquisition. When it is necessary to synchronize the live-time clocks in the ADCs with the data acquisition in the Model HM413, the "I" command can be used to start and stop data acquisition simultaneously on all modules in the same crate. Front-panel LEDs indicate when the HM413 is enabled to accept data, when data is accepted for histogramming, and when a CAMAC communication is occurring.

CAMAC commands are also provided for configuring the FERAbus functions.

CAMAC readout of selected memory segments proceeds as a block transfer in the Q-Stop mode. For ADC identification, the first channel of a segment readout contains the Segment Number and the Virtual Station Number of the ADC. A LAM output can be used to signal the need for readout when the counts in one of the memory channels have exceeded the memory capacity.

The Model HM413 automatically solves the problem of the "occasionally missing readout request" in the Coincidence

mode. When a standard FERAbus system operates in the zero-suppressed readout mode, the master GATE from the readout controller (e.g., LeCroy 4301 FERA Driver) signals the ADCs to analyze the coincident events at their inputs, and to wait for a common Clear (CLR) after readout. Occasionally, all of the ADCs produce a zero response, because they fail to detect any analog input signals. In this case, no readout request is generated, and the standard readout controller will not produce the Clear signal required to release the ADCs for the next event. The Model HM413 detects this situation, and prevents lock-up by initiating a readout request 10  $\mu$ s after the end of the master GATE signal. The readout controller responds to the readout request by issuing a readout command, which results in a CLR signal being generated.

To facilitate making the interconnections between the FERAbus modules, the C-ECLBUS Cable Kit is recommended as a separately ordered accessory. This kit contains the cables and connectors needed for a crate full of FERAbus modules.

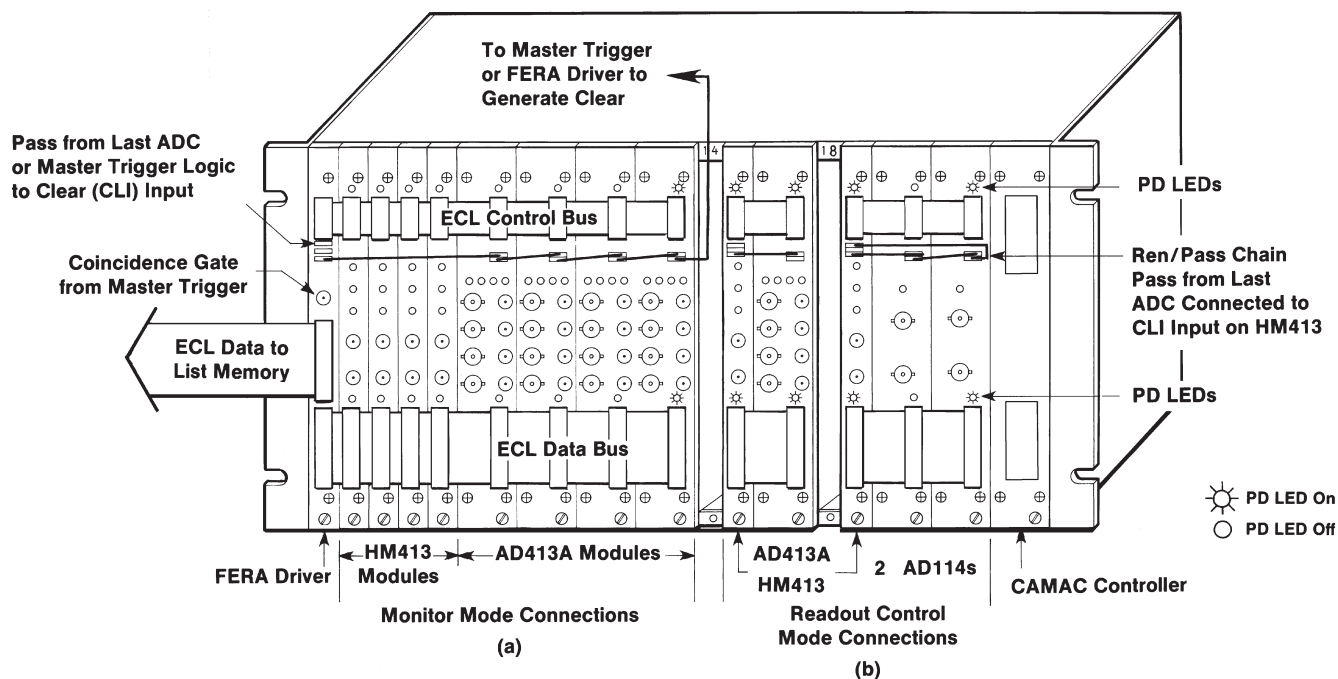


Fig. 1. Interconnection of the Model HM413 with FERAbus ADCs for (a) the Monitor mode, and (b) the Readout Control mode.

# HM413

## CAMAC FERAbus Histogramming Memory

### Specifications

#### PERFORMANCE

**OPERATING MODES** To provide the Virtual Station Number and Subaddress information required by the Model HM413, all FERAbus ADCs must operate in the zero-suppressed readout mode.

**Monitor Mode** The Model HM413 histograms spectra from preselected ADCs while listening to list-mode readouts on the FERAbus. The LeCroy 4301 FERA Driver functions as the readout controller (Fig. 1a). Typically used for multi-parameter coincidence measurements, with multiple ADCs providing list-mode readout. Accepts either Coincidence- or Singles-mode readout.

**Readout Control Mode** The Model HM413 operates as the readout controller for histogramming *singles* spectra from several ADCs (Fig. 1b). Data acquisition can be gated or ungated.

#### CAMAC-CONTROLLED FUNCTIONS

Histogramming start/stop, readout of selected segments, clear memory, ADC/segment assignments, and FERAbus functions.

**MEMORY LENGTH** 32,768 channels.

**MEMORY CAPACITY** 24 Bits (16,777,215 counts per channel).

#### PROGRAMMABLE MEMORY

**CONFIGURATIONS** Two 16,384-channel segments, four 8192-channel segments, eight 4096-channel segments, sixteen 2048-channel segments, or thirty-two 1024-channel segments. Selected by CAMAC commands to match the ADCs being histogrammed.

**FERAbus DATA TRANSFER RATE** 100 ns per word.

#### MAXIMUM NUMBER OF ADCs ON THE FERAbus

One CAMAC crate full of ADCs in the Monitor mode. Limited to the ADCs specified by the segment assignments in the Readout Control mode.

#### OPERATING TEMPERATURE RANGE

0 to 50°C.

#### CONTROLS AND INDICATORS

**CONTROL SIGNAL SWITCH** The DIP switch on the printed circuit board serves two functions: (a) disconnection of the CLR, GATE, and WAK outputs from the ECL Control Bus, and (b) switching the cable termination for the REQ signal. Position assignments and settings are in Table 1.

**FAST NIM/TTL LOGIC JUMPERS** Two circuit-board jumpers select the logic convention for the GAI and CLI LEMO inputs. The fast negative NIM logic position is towards the front of the module; the TTL position is towards the rear. Each jumper controls the input attached to the adjacent coaxial cable.

**PD** Two front-panel red LED indicators (one for the ECL CONTROL connector, and one for the ECL DATA connector) are turned ON when the ECL pull-down resistors are installed for the ECL CONTROL connector, or when the termination resistors are installed for the ECL DATA connector. See ECL Inputs/Outputs.

**ANALYZE** Front-panel LED indicates that the Model HM413 is enabled to process data from the ADCs.

**STORED** Front-panel LED flashes for approximately 1 ms each time valid data is identified and stored in the appropriate memory segment. The relative brightness indicates the rate at which events are being stored.

**CAMAC READ** Front-panel LED indicates that a CAMAC read or write communication is in progress.

#### INPUTS

**GAI** Front-panel LEMO connector accepts the master GATE signal for distribution to the ADCs on the ECL Control bus. See GATE description for function. A circuit-board jumper selects NIM-standard fast negative logic (50-Ω input impedance), or TTL logic (also compatible with NIM-standard positive logic; 1-kΩ input impedance). The LEMO GAI input is OR'ed with the ECL GAI input.

**CLI** Front-panel LEMO connector accepts the Clear Input (CLI) signal for distribution to the ADCs as the CLR signal on the ECL CONTROL bus. See the CLI description under ECL Inputs/Outputs for functional definition. A circuit-board jumper selects NIM-standard fast negative logic (50-Ω input impedance), or TTL logic (also compatible with NIM-standard positive logic; 1-kΩ input impedance). The LEMO CLI input is OR'ed with the ECL CLI input.

#### ECL INPUTS/OUTPUTS

FERAbus communication with the ADCs utilizes ECL logic levels on the front-panel CONTROL and DATA connectors. All pull-down and termination resistors must be removed from the Model HM413 when operating in the Monitor mode, and installed when operating in the Readout Control mode (see PD LED, CONTROL SIGNAL SWITCH, and Fig. 1). Only one ADC on each ECL bus should have the pull-down and termination resistors installed. The termination resistors are normally installed at the receiving end for each pair of ECL signal lines. The CLI, GAI, and REO connectors require construction of 100-Ω, twisted-pair cables, with a 2-pin socket and housing (AMP 1-87756-8 and AMP 5-87456-3) on each end.

**ECL LOGIC LEVELS** The nominal ECL logic levels (into a 100-Ω differential load) are:

	Left (+) Pin	Right (-) Pin
Logic 0	-1.8 V	-0.9 V
Logic 1	-0.9 V	-1.8 V

For single-ended operation (-) pin is grounded in the receiving module.

**ECL DATA INPUT** Front-panel, 17- by 2-pin connector (AMP 1-103326-7) accepts the digitized ADC outputs in the form of single-ended ECL signals from the ECL Data Bus. Up to 16 parallel bits can be accepted and stored into the FIFO memory at the time of the Write Strobe (WST) signal. Bits are sequentially assigned, with bit 1 assigned the two pins in row 1 and bit 16 occupying the two

Table 1. Control Signal Switch.

	SIGNAL							
	REQ		CLR		GATE		WAK	
	-	+	-	+	-	+	+	-
Switch Position Number	1	2	3	4	5	6	7	8
Cable Termination	ON	ON	-	-	-	-	-	-
No Termination	OFF	OFF	-	-	-	-	-	-
Outputs Connected	-	-	ON	ON	ON	ON	ON	ON
Outputs Disconnected	-	-	OFF	OFF	OFF	OFF	OFF	OFF

Set all Switches: OFF for the Monitor mode, ON for the Readout Control mode

pins in row 16. Row 17 is not connected. Interconnection between the Model HM413 and other modules utilizing the ECL Data Bus requires the construction of a 34-conductor ribbon cable (3M part number 3365/34) with 17- by 2-pin headers (3M 3414-6006 or AMP 499498-9) spaced to match the configuration of modules. Two removable termination resistor packs provide 100-Ω input impedances on the (+) inputs for the Readout Control mode. The readout from the ADCs on the ECL Data Bus must conform to the following format. Each ADC must operate in zero-suppression mode and deliver 2 to 17 data words during readout. The first is always a header word:

B16	B15	.....	B12	B11	B10	B9	B8	.....	B1
1	WRDCNT		0	0	0				VSN

followed by 1 to 16 data records, each with the format:

B16	B15	.....	BN	B(N-1)	.....	B1
0	SUBADDR					DATA

according to the following definitions:

**B16** The Model HM413 uses bit 16 to distinguish header words from data records. For a header word B16 = 1. For a data word B16 = 0.

**WRDCNT** The word count is a value from 0 to 15, which defines the number of data records that follow in the readout. The WRDCNT information is not used by the Model HM413.

**VSN** The Virtual Station Number (0–255) identifies the ADC module number during zero-suppressed readout. The Model HM413 uses the VSN to identify the ADC data it must histogram.

**BN, BN-1** The value of N is determined by the maximum subaddress provided by the ADC module (number of ADC inputs per module).

ADC Inputs per Module:	1	2	4	8	16
BN:	B15	B15	B14	B13	B12

**SUBADDR** The subaddress identifies the individual ADC within the module having the VSN designated in the header word. The Model HM413 decodes the SUBADDR to histogram ADCs in their sequentially assigned segments of memory.

**DATA** The conversion data from the ADC identified by the SUBADDR and VSN. The number of bits of data depends on the number of ADC inputs per module and the number of bits in the individual ADCs.

**ECL CONTROL BUS** The 8- by 2-pin connector at the top of the front panel accommodates the ECL Control Bus for synchronizing data acquisition among multiple ADCs, and for controlling ECL data transfer. A row of two pins is assigned to each differential ECL input or output, with the top 8 rows forming the ECL Control Bus. Interconnection between ADC modules and the Model HM413 requires the construction of a 16-conductor ribbon cable (3M part number 3356/16) with 8- by 2-pin headers (3M 3452-6006 or AMP 499497-3) spaced to match the configuration of modules. The logic signals in the ECL Control Bus are listed below. If a LeCroy 4301 FERA Driver is connected to the bus, the CLR, GATE, and WAK output drivers in the Model HM413 must be disconnected from the ECL Control Bus by the CONTROL SIGNAL SWITCH for operation in the Monitor mode.

**N/C** No connection.

**WST** The Write Strobe input is provided by the ADC presenting data for readout on the bus. WST indicates when each word on the ECL Data Bus is valid, and causes the Model HM413 to read the word into a FIFO memory. The leading edge of the WST pulse must fall inside the data pulse and must arrive at least 10 ns after the data are valid. The minimum WST width is 40 ns. Minimum data transfer time is 100 ns/word. The 100-Ω termination resistor (R7) on the (+) input must be removed for the Monitor mode, and installed for the Readout Control mode. The (–) input is always grounded.

**REQ** The readout Request signal is both an ECL input and an ECL output on the Model HM413. When an ADC has data ready for readout, the ADC issues an REQ signal. The Model HM413 recognizes the REQ signal, waits for a fixed delay (factory set to 200 ns), then issues the REO signal on a separate connector. In the Readout Control mode, the REO signal is connected to the Readout Enable (REN) input on the first ADC in the readout chain to initiate the the readout sequence. The REO signal is not used in the Monitor mode. In either mode, the Model HM413 monitors the master GATE and CLR lines on the ECL Control Bus. If a CLR signal is not detected within 10 μs of the end of a master GATE signal, the Model HM413 will generate an REQ signal. This initiates a readout cycle, which generates a CLR, thus preventing lock-up of the analyze/ readout cycle when none of the ADCs detected an event. REQ is terminated by the CLR signal. The REQ output can be enabled for the Coincidence mode by the F(26)-A(2) CAMAC command, or disabled for the Singles mode by the F(24)-A(2) command. Terminations of 100

Ω on the (+) input and ground on the (–) input must be connected by the CONTROL SIGNAL SWITCH for the Readout Control mode.

**CLR** In the Readout Control mode, the CLR output is issued by the Model HM413 at the end of ADC readout. This signal clears the ADCs and releases them to analyze the next event. Normally, the CLR signal is generated by connecting the PASS signal from the last ADC in the readout loop to the CLI input on the Model HM413. The CLR signal can also be generated by the CAMAC command F(9)-A(1). The CLR connector on the Model HM413 serves as an ECL input and an ECL output. The input function contains no termination resistors. For the Monitor mode, the CLR output and its pull-down resistors must be disconnected by the CONTROL SIGNAL SWITCH. In the Readout Control mode, the CLR output is enabled for the Coincidence mode by the F(26)-A(2) CAMAC command, or disabled for the Singles mode by the F(24)-A(2) command.

**GATE** The master GATE output is distributed to all ADCs connected to the ECL Control Bus for gating in the Readout Control mode. The GATE output is an ECL version of the input provided to the Model HM413 on the GAI connector. The logic 1 state enables acceptance of analog inputs by the ADCs for conversion, and forces all ADCs to wait for a common Clear (CLR) after readout. The master GATE signal is not required by ORTEC ADCs operating in the Singles mode. The GATE connector on the Model HM413 serves as an ECL output and an ECL input (see REQ). The input function contains no termination resistors. For the Monitor mode, the GATE output and its pull-down resistors must be disconnected by the CONTROL SIGNAL SWITCH. In the Readout Control mode, the GATE output is enabled for the Coincidence mode by the F(26)-A(2) CAMAC command, or disabled for the Singles mode by the F(24)-A(2) command.

**WAK** The Write Acknowledge output is used only in the Readout Control mode. When an ADC has data ready for transfer on the ECL Data Bus, it issues a Write Strobe (WST) signal on the ECL Control Bus. After a 35-ns delay, the Model HM413 responds with a 40-ns-wide WAK signal. The WAK signal indicates completion of the transfer, and enables the next word to be asserted on the bus by the ADCs. For the Monitor mode, the WAK output and its pull-down resistors must be disconnected by the CONTROL SIGNAL SWITCH.

# HM413

## CAMAC FERAbus Histogramming Memory

**GND** Both pins connected to ground.

**ROW 8** No connection.

**CLI** Front-panel 1- by 2-pin connector accepts the Clear Input (CLI) signal for distribution to the ADCs as the CLR signal on the ECL Control Bus. The ECL CLI input is OR'ed with the LEMO CLI input. At the end of ADC readout, a logic 1 signal is applied to clear the ADCs and release them to accept the next event. CLI is normally derived from the PASS output of the last ADC in the readout loop. CLI is required in the Readout Control mode with LeCroy 4300B ADCs, and ORTEC ADCs set to the Coincidence mode. CLI is not required by the Model HM413 with ORTEC ADCs set to the Singles mode, or all ADCs in the Monitor mode. Differential input impedance is nominally 100  $\Omega$ .

**GAI** Front-panel 1- by 2-pin connector accepts the master GATE signal for distribution to the ADCs on the ECL Control Bus. See GATE description for function. Differential input impedance is nominally 100  $\Omega$ . The ECL GAI input is OR'ed with the LEMO GAI input.

**REO** Front-panel 1- by 2-pin connector provides the Readout ECL output for initiating readout at the REN input on the first ADC in the readout loop. REO is used only in the Readout Control mode. See REQ description for function. The CONTROL PD LED is on when the REO pull-down resistors are installed for operation in the Readout Control mode.

**N/C** No connection.

### CAMAC COMMANDS

- Z** Initializes the module. Clears the LAM flip-flop, disables data collection, sets all registers to zero, disables the Coincidence mode, and clears the data memory to zero. The Q response is inhibited while the memory is being cleared.
- I** Inhibits the Store function as long as the I signal is present. Used to stop and start data acquisition simultaneously for all ADCs and HM413 modules in the same crate.
- X** The module responds with X = 1 for all valid function commands.
- Q** The module responds with Q = 1 if the function command can be executed when issued.
- L** A LAM is generated when the content of any channel exceeds the capacity of the memory. Active only if the LAM is enabled [see F(24)·A(0) and F(26)·A(0)].

**F(0)·A(0)** Initiates reading the entire memory segment (as specified by the Segment Register) in the Q-Stop mode. Reads the 24-bit (R1 to R24) data word at the current memory address, and increments the address by one at S2. A Q = 0 response is generated when the address pointer exceeds the current segment block while reading a segment. The Segment Register must be loaded by the F(17)·A(3) command before reading memory. Load segment 1 through 32 (depending on the number of segments selected) to read the desired segment. The data for the first channel in the readout is replaced with a word that contains the Segment Number in bits 9 to 16 and the Virtual Station Number for the segments in bits 1 to 8. Subsequent words contain the channel-by-channel histogram data for the segment.

**F(1)·A(0)** Reads the Configuration Register (R1 to R5).

**F(8)·A(0)** Tests LAM. Q = 1 if LAM is present.

**F(9)·A(0)** Causes the Model HM413 to clear the contents of every channel of memory to a value of zero. This takes approximately 5 ms. No Q responses will be generated for further commands while clearing memory. Segment 0 must be selected via F(17)·A(3) before issuing F(9)·A(0).

**F(9)·A(1)** Generates a Clear signal (CLR) on the ECL Control Bus, if positions 3 and 4 of the CONTROL SIGNAL SWITCH are set ON for the Readout Control Mode.

**F(10)·A(0)** Tests and clears LAM. A Q = 1 response is generated if a LAM is present and the LAM is cleared.

**F(16)·A(0)** Writes the memory address (W1 to W15) to be read by a subsequent F(0)·A(0) command.

**F(17)·A(0)** Writes to the VSN1 Register (W1 to W8).

**F(17)·A(1)** Writes to the VSN2 Register (W1 to W8).

**F(17)·A(2)** Writes to the Configuration Register (W1 to W5).

**F(17)·A(3)** Writes to the Segment Register (W1 to W8).

**F(24)·A(0)** Disables LAM.

**F(24)·A(1)** Stops the Analyze mode (data histogramming). Data transfer on the ECL Data Bus continues, independent of this command.

**F(24)·A(2)** Disables the Coincidence mode for operation in the Singles mode. Disables the generation of REQ by the Model HM413 following the termination of the master GATE signal. Also disables the CLR and GATE output signals. The Z command also disables the Coincidence mode.

**F(26)·A(0)** Enables LAM. LAM is generated when any channel exceeds the capacity of the memory.

**F(26)·A(1)** Starts the Analyze mode (data histogramming).

**F(26)·A(2)** Enables the Coincidence mode. Enables the master GATE and CLR outputs. Enables the generation of an REQ signal by the Model HM413 if a CLR signal is not detected within 10  $\mu$ s after the GATE signal is terminated (see the REQ description).

### REGISTERS

**VSN1 REGISTER** The Virtual Station Number of the ADC module that the Model HM413 will histogram in the first half of memory must be written into this register. This value is compared to the virtual station number in the header words from the ADCs to determine whether the Model HM413 should respond to the data. In some cases the ADC with VSN1 will occupy the entire data memory. The command F(17)·A(0) writes to the VSN1 Register (W1 to W8). To accept data, the VSN1 comparator must always be enabled (see Configuration Register).

**VSN2 REGISTER** The function of this register is the same as the VSN1 Register, but it allows the data from two separate modules to be processed. The data that matches this register will be placed in the top half of the data memory. The command F(17)·A(1) writes to the VSN2 Register (W1 to W8). The VSN2 comparator must be disabled when the ADC with VSN1 occupies the entire data memory (see Configuration Register).

**CONFIGURATION REGISTER** The Configuration Register is a 5-bit register that allows the operator to enable the VSN (Virtual Station Number) comparators for ADC identification, and select the number of segments that the data memory is divided into.

Command F(1)-A(0) reads, and F(17)-A(2) writes to the Configuration Register. The bit assignments are:

Bit	Function
1	Disable 1st VSN comparator. Enable = 0, disable = 1. Must always be enabled in order to accept ADC data.
2	Disable 2nd VSN comparator. Enable = 0, disable = 1. Must be disabled when the entire memory is assigned to a single VSN (i.e., a single ADC module).
3	Segment select 1
4	Segment select 2
5	Segment select 3

} See Segment Assignments

### Segment Assignments

Configuration Register Bits			Number of Segments	Channels per Segment
5	4	3		
0	0	0	2	16,384
0	0	1	4	8,192
0	1	0	8	4,096
0	1	1	16	2,048
1	0	0	32	1,024

**SEGMENT SELECT REGISTER** This register allows the operator to select an individual segment for readout by loading the number of the segment (1 to 32). Care should be taken not to load a value greater than the number of segments selected by the Configuration Register. Segments are sequentially assigned in the order of the ADC Subaddress numbers. The command F(17)-A(3) writes to the Segment Select Register (W1 to W8).

### ELECTRICAL AND MECHANICAL

**POWER REQUIRED** The Model HM413 derives its power from a CAMAC crate supplying  $\pm 6$  V. The power required is +6 V at 2.1 A, -6 V at 1.0 A.

### WEIGHT

**Net** 0.81 kg (1.8 lb).

**Shipping** 1.8 kg (4.0 lb).

**DIMENSIONS** CAMAC-standard single-width module, 1.70 X 22.15 cm (0.67 X 8.72 in.) front panel per IEEE/583-1982 (Reaff 1988).

## Optional Accessories

The C-ECLBUS Cable Kit is recommended as an accessory to facilitate the FERAbus interconnections. Each kit contains:

Quantity	Description
1	16-conductor ribbon cable with 23 headers installed at 7.6-cm intervals for the ECL Control Bus.
1	34-conductor ribbon cable with 23 headers installed at 7.6-cm intervals for the ECL Data Bus.
1	51-cm long twisted pair cable with 2-pin sockets and headers on each end for the PASS to CLI connection.
23	15-cm long twisted pair cables with 2-pin sockets and headers on each end for the REO to REN, and the PASS to REN connections.

The ribbon cables will serve an entire crate full of FERAbus modules, and can be cut to handle smaller groups of modules.

## Ordering Information

To order, specify:

Model	Description
<b>HM413</b>	CAMAC FERAbus Histogramming Memory
<b>C-ECLBUS</b>	Cable Kit for the ECL Bus

## Application Addendum

The Model HM413 is compatible with the following LeCroy modules for readout on the FERAbus™.

4300B	16-Input Fast Encoding & Readout Charge ADC
4301	Fast Encoding & Readout Driver Module
4302	Dual Port Memory
3341	8-Input, 12-Bit Charge-Integrating ADC
3351	8-Input, 12-Bit Peak-Sensing ADC
3371	8-Input, 12-Bit TDC
3377*	Drift Chamber Time-to-Digital Converter

\*When operating the LeCroy 3377 on the FERAbus (ECLbus) with the HM413, the "4300B mode" and the "Single-Word Readout Mode" must be selected in the 3377. This allows the HM413 to histogram the thirty-two separate time digitizers in the 3377 with 10-bit time resolution.

A special setup is also required on the HM413 to accommodate thirty-two spectra of 1k length from a single 3377 module (single Virtual Station Number). Set the HM413 to process 4 spectra of 8k length. The subaddress bits supplied by the 3377 will ensure that the thirty-two 1k spectra get stored in the right locations in the HM413 memory. The HM413 memory must subsequently be read into the computer memory as four blocks of 8k length. In the computer one can readily pull out the individual 1k spectra.

The 3377 can deliver more than 32 data words for a single START trigger, because the 3377 can record multiple STOP events for a single START pulse. This is no problem for the HM413. The HM413 identifies a header word by noting that bit 16 is set to 1. The Virtual Station Number (VSN) included in the header word is captured by the HM413 and compared to the VSN the HM413 has been told to accept for histogramming. If the comparison results in a match, the HM413 histograms all subsequent data words until a new header word is detected. Data words are identified by bit 16 being set to zero.

FERAbus™ is a trademark of the LeCroy Corporation.

**HM413**  
CAMAC FERAbus Histogramming Memory

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# HM413

## CAMAC FERAbus Histogramming Memory

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Specifications subject to change  
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